

Appl. No. 10/605,521  
Amdt. dated November 17, 2004  
Reply to Office action of August 18, 2004

### AMENDMENTS TO THE CLAIMS

1. (currently amended) A printed circuit inductor of a printed circuit board with at least a first wiring layer and a second wiring layer comprising:
- 5       a first conductive trace formed on a first wiring layer of a printed circuit board;  
      a second conductive trace formed on a second wiring layer of a printed circuit board, wherein the second layer is disposed below and parallel to the first layer, the layers being separated by an insulating material;  
      a third conductive trace formed on the first wiring layer and parallel to the first  
10       conductive trace;  
      a fourth conductive trace formed on the second wiring layer and parallel to the second conductive trace;  
      a first via plug directly connected to a first end of the first conductive trace and to a first end of the second conductive trace;  
15       a second via plug directly connected to a second end of the second conductive trace and to a first end of the third conductive trace; and  
      a third via plug directly connected to a second end of the third conductive trace and a to first end of the fourth conductive trace;  
      wherein the first via plug, the second via plug and the third via plug are positioned  
20       along two parallel lines; or the first via plug, the second via plug and the third via plug are aligned but not positioned along two parallel lines; or the first via plug, the second via plug and the third via plug are not aligned
2. (original) The inductor of claim 1 wherein the first via plug is perpendicular to the first  
25       conductive trace, the second via plug is perpendicular to the second conductive trace, and the third via plug is perpendicular to the third conductive trace.
3. (currently amended) A printed circuit inductor of a printed circuit board with a

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plurality of wiring layers comprising:

- 5 a plurality of conductive traces formed on a plurality of wiring layers of a printed circuit board, wherein ~~the~~ a conductive element of ~~the~~ a printed circuit inductor is formed from interconnected conductive traces disposed on separate wiring layers, each conductive trace having at least an end disposed coincident with an end of a conductive trace disposed on a separate layer allowing interconnection by a via;
- 10 a plurality of insulating layers for isolating the conductive layers from each other; and
- a plurality of via plugs each directly connecting the conductive traces on different conductive layers;
- 15 wherein the plurality of via plugs are positioned along two parallel lines; or the plurality of via plugs are aligned but not positioned along two parallel lines; or the plurality of via plugs are not aligned.

4. (original) The inductor of claim 3 wherein the plurality of conductive layers is formed having two layers.
- 20 5. (original) The inductor of claim 3 wherein the plurality of via plugs is perpendicular to the plurality of conductive layers.
6. (original) The inductor of claim 3 wherein the magnetic field generated by the inductor is in parallel with the conductive layers.
- 25 7. (New) The printed circuit inductor of claim 1, wherein conductive traces formed on the first wiring layer are skewed symmetrically with respect to conductive traces formed on the second wiring layer

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- 5 8. (New) The printed circuit inductor of a printed circuit board of claim 3, wherein one end of each conductive trace is directly connected to one end of a corresponding conductive trace formed on a separate wiring layer through one of the plurality of via plugs, and wherein the conductive traces formed on a first separate wiring layer are parallel to each other and skewed symmetrically with respect to the corresponding conductive traces formed on a second separate wiring layer, the traces formed on the second separate wiring layer being parallel to each other

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